processor for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

selects a first memory circuit and generates a write-address for the first memory circuit for a data belonging to the set of input data;

selects a second memory circuit and generates a read-address for the second memory circuit for a data belonging to the set of output.

REMARKS

Reconsideration and allowance of all the pending claims are respectfully requested in light of the above amendments and the following remarks.

Claims 1-5 remain pending herein.

SUMMARY OF THE REJECTIONS

I. Claims 1-5 are objected to because of an informality in Claim 1.

II. Claims 1-5 stand rejected under 35 U.S.C.§102(b) as allegedly being anticipated by Torrii et al. (U.S. 4,734,850, hereafter "Torii").

APPLICANT'S TRAVERSAL

I. Claim 1 has been amended to overcome the informality cited in the Final Office Action.

II. Claims 1, 4 and 5 have been amended to clarify that the memory system comprises *independent* memory circuits, support for which is provided in the specification at least at page 3, lines 31. In addition, the plurality of independent memory circuits of the memory system 2, which are shared by both the first processor and the second processor (as shown in Figs. 1 and 2, and described at least at page 3, lines 25-28 of the specification), are set up by the master controller.

In contrast, Torii fails to disclose or suggest a single master controller that sets up the plurality of independent memory circuits of the memory system.

It is respectfully submitted that Torii (please see Fig. 2) discloses a plurality of execution units (4,5,6,) each having *respective* mode indicating circuits for corresponding FIFO memories (20,21,22). A Mode Indicating Circuit 41 (shown in Fig. 2) controls the read and write banks of a single FIFO memory. It is also respectfully

submitted that Torii discloses at column 2, lines 62-66 that Fig. 2 depicts "any one of FIFO memories 20, 21 and 22 shown in Fig. 1." Thus, Torii discloses that each FIFO has an individual Mode Indicating Circuit 41 that controls only that particular FIFO.

Accordingly, claims 1-5 are not anticipated by Torii because this reference fails to disclose all of the elements recited by the instant claims.

As stated in MPEP 2131, in order for a reference to anticipate, each and every element must be disclosed in a single reference.

Moreover, the Court of Appeals held in *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628,631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) that:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

It is respectfully submitted that in the rejection of instant claims 1-5 should be withdrawn because the Torii reference fails to disclose all the elements recited in Applicant's claims. It is also respectfully submitted that none of the instant claims would have been obvious to a person of ordinary skill in the art in view of Torii.

For all the foregoing reasons, it is respectfully submitted that all of the present claims are patentable in view of the cited reference. A Notice of Allowance is respectfully requested.

Should the Examiner deem that there are any issues which may be best resolved by telephone communication, he is respectfully requested to telephone Applicant's undersigned Attorney at the number listed below.

Respectfully submitted,
Tony Piotrowski
Registration No. 42,080

Date: 12/12/01

By: Stephen Gigante
Attorney for Applicant
Registration No. 42,576

Enclosures:
Marked-Up Version to Show Changes Made
Notice of Appeal

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Inventors : Marc DURANTON Art Unit: 2185

Application No.: 09/316,560 Examiner: R. BRAGDON

Filed : May 24, 1999

For : DATA PROCESSING ARRANGEMENT AND MEMORY SYSTEM

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Assistant Commissioner for Patents
U.S. Patent and Trademark Office
Box AF
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated September 12, 2001, please note the following marked up changes to the specification and claims:

AMENDMENT
VERSION WITH MARKINGS TO SHOW CHANGES MADE
Application No. 09/316,560 Atty Docket F99540

IN THE CLAIMS:

1. (Twice Amended) A data processing arrangement comprising:

a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system comprising a plurality of independent memory circuits shared by the first processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data;

a master controller for setting up the plurality of independent memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit for, on the basis of the control commands, selecting a first memory circuit and generating a write-address for the first memory circuit when a data from the set of

input data provided by the first processor, and for, on the basis of the control commands, selecting a second memory circuit and generating a read-address [in] for the second memory circuit when a data from the set of output data is required by the second processor.

4. (Twice Amended) A memory system comprising:

a plurality of independent memory circuits for receiving successive sets of input data and for providing successive sets of output data;

a control unit being programmable by means of control commands associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a write-address for the first memory circuit, when a data from the set of input data is received, and for selecting a second memory circuit and generating a read-address for the second memory circuit, when a data from the set of output data is provided.

5. (Twice Amended) A method of processing data in a data

processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of independent memory circuits shared by both the first processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

selects a first memory circuit and generates a write-address for the first memory circuit for a data belonging to the set of input data;

selects a second memory circuit and generates a read-address for the second memory circuit for a data belonging to the set of output data.